YM3616

Signal Processor & Controller for Compact Disc Players (SPCII)

OUTLINE

The YM3616 single-chip CMOS Signal Processor and Controller LSI incorporates all the signal processing and servo control functions required to design a state-of-the-art compact disc (CD) player.

In addition to EMF signal demodulation, error detection and correction, the YM3616 provides intelligent control of the focus, disc motor, tracking and feed servos.

High-speed track search is implemented using a built-in counter that tallies the number of tracks traversed. Conventional search functions are also available.

Both MSB first and LSB first outputs are supported, facilitating an interface to either type of DAC. Further, when used in conjunction with the YM3404 Digital Filter and YM3613 Digital Interface, the YM3616 is the ideal choice for advanced, high-reliability CD player designs. The YM3616 is available in 80-pin plastic flat packs.

FEATURES

- 8.6436MHz external clock signal generates the reference clock and all internal timing signals.
- Clock regeneration and sync signal separation based on EFM signal. EFM signal demodulation.
- Q-subcode separation and CRC checking. EIAJ output format.
- Disk motor control using playback and reference clock signal differential.
- Control of servo functions such as tracking and feed for track selection and fast forward search, using command inputs from microcontroller.
- Built-in track counter for high-speed track searches
- EFM demodulation signal buffering using external RAM absorbs jitter caused by uneven disc rotation. Up to ±4 frames can be buffered.
- EFM demodulation signal reordering using unscrambling and de-interleaving
- Single-error detection and correction and error flag processing (double-error correction)
- MSB first or LSB first outputs
- Error flags outputs for CD/ROM or other digital I/O systems
- Low-power silicon-gate CMOS process
- 80-pin flat pack (QFP)

YM3616カタログ
CATALOG No. : LSI-[illegible]
1988

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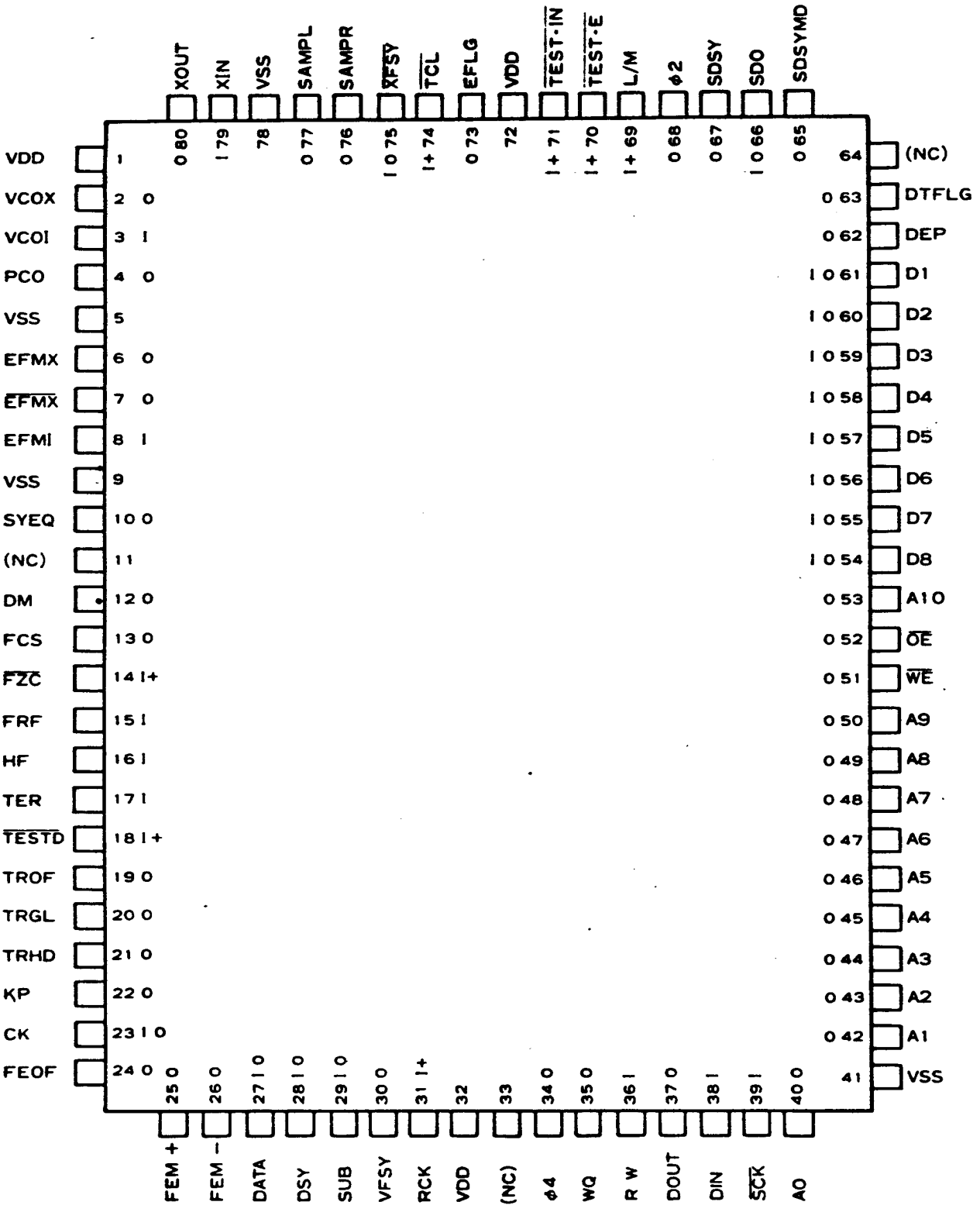
PINOUTS



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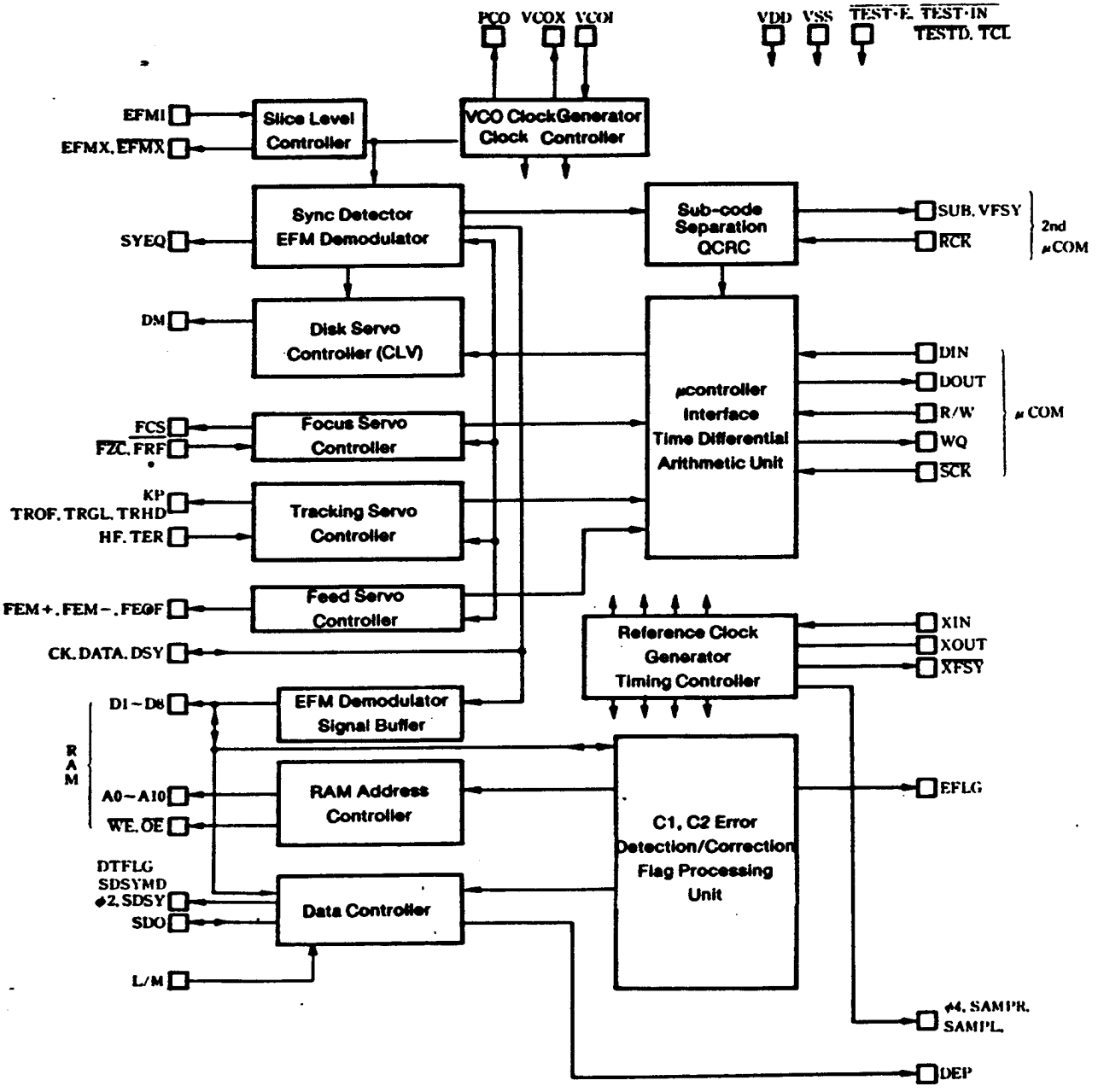
BLOCK DIAGRAM



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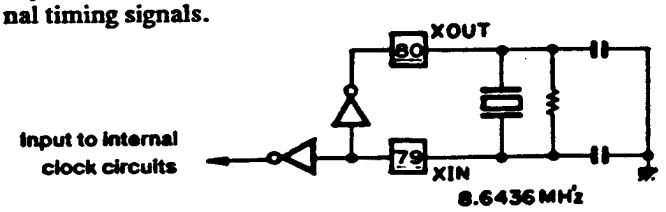
PIN FUNCTIONS

1. **Clock Signal**

   XIN & XOUT (Pins 79 & 80)

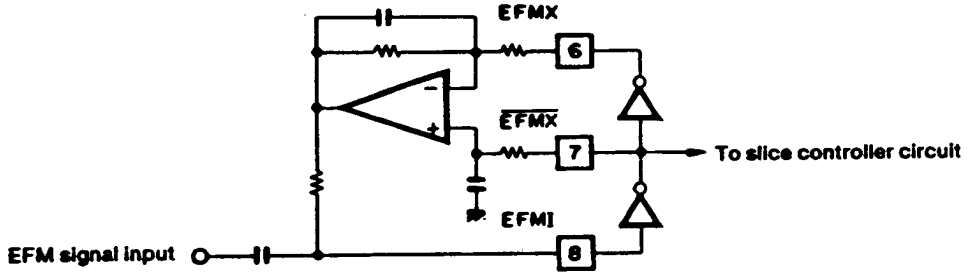
   Connecting a crystal oscillator (8.6436MHz) between XIN and XOUT and 20pF capacitors between both pins and GND generates the reference clock and all internal timing signals.



2. **EFM Signal External Circuit**

   EFMI, $\overline{\text{EFMX}}$, EFMX (Pins 8, 7 & 6)

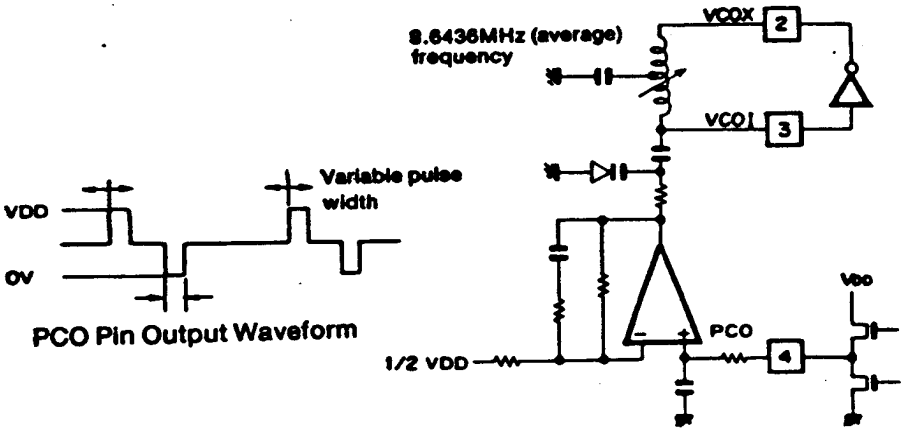
   The 1 to $2V_{PP}$ signal from the optical pickup is input at EFMI. Amplitude limited signals with inverted phase are generated at $\overline{\text{EFMX}}$ and EFMX and used to perform slice level control.



3. **Clock Regeneration Circuit**

   PCO, VCOI & VCOX (Pins 4, 3 & 2)

   Connecting an LC resonator between VCOI and VCOX generates an 8.6436MHz (average) clock signal. The output at PCO is the phase difference when there is a polarity change in the clock and EFM pattern, and the polarity of the varicap diode is set so that the frequency rises when positive to perform clock regeneration.



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4. **In-Sync Signal**

SYEQ (Pin 10)

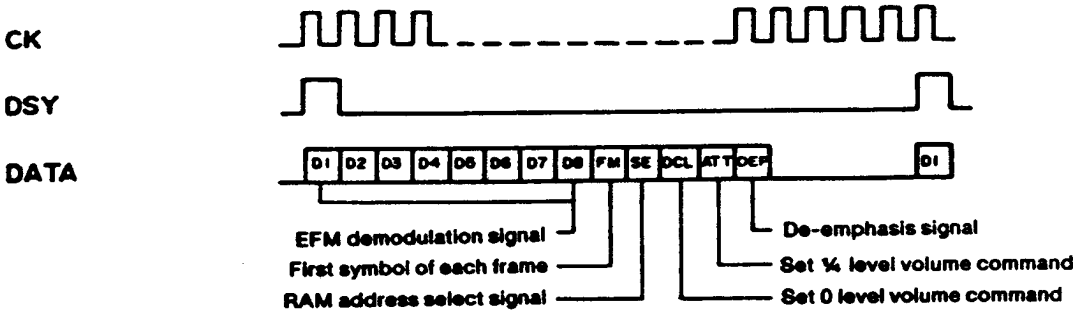
Check output. HIGH when the sync signal detected from the EFM pattern is in sync with the internal counter sync signal.

5. **EFM Demodulation Signal Check Output**

CK, DATA & DSY (Pins 27, 28 & 29)

CK is the 4.3218MHz (average) clock signal obtained by binary prescaling VCO. DATA is the 17-bit CK bit-rate serial signal containing the 8-bit EFM demodulation signal and 5-bit data control signal. DSY is a sync signal which goes HIGH with the same timing as the first CK signal.

Together, CK, DATA and DSY are used to check the EFM demodulation signal.

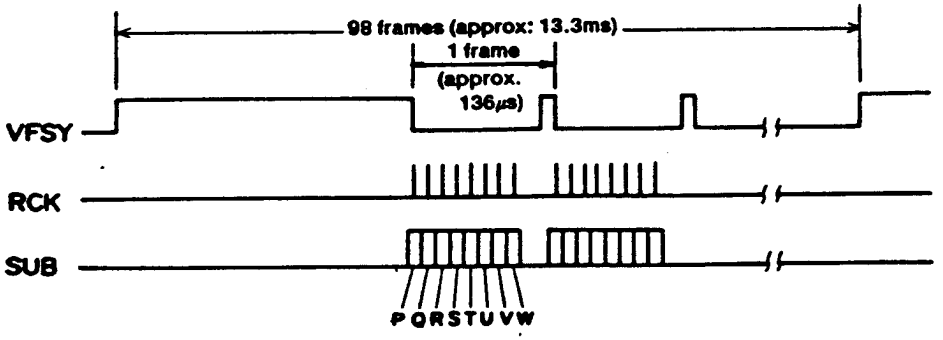


6. **Subcodes**

- SUB, VFSY & RCK (Pins 29, 30 & 31)

VFSY is a composite sync signal output for the data and subcode frames (a total of 98 frames). Subcodes P through W are output in serial format at SUB by detecting the VFSY signal level change (HIGH to LOW) externally, and sending 8 clock pulses to RCK.

SUB, VFSY and RCK conform to the EIAJ subcode interface standard.



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7. **Q-Code Output**

WQ, R/W, DOUT & $\overline{SCK}$ (Pins 35, 36, 37 & 39)

Contents of DOUT

	Internal Status	
1		
2	CONT	ADR
3	TNO	
4	X	
5	MIN	
6	SEC	
7	FRAME	
8	P-CODE	
9	A-MIN	
10	A-SEC	
11	A-FRAME	

Contents of Internal Status Register

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SIGN	S2	S1	8F	4F	MZ	FCO	NQ

IGN Search polarity
S1, S2 Search mode
4F, 8F Frame error
MZ 1 when disc motor.is stopped.
FCO 1 when out of focus.
NQ 1 when new Q-code is written.

D_7 is 1 and D_6 to D_3 are 0 when track counting is completed.

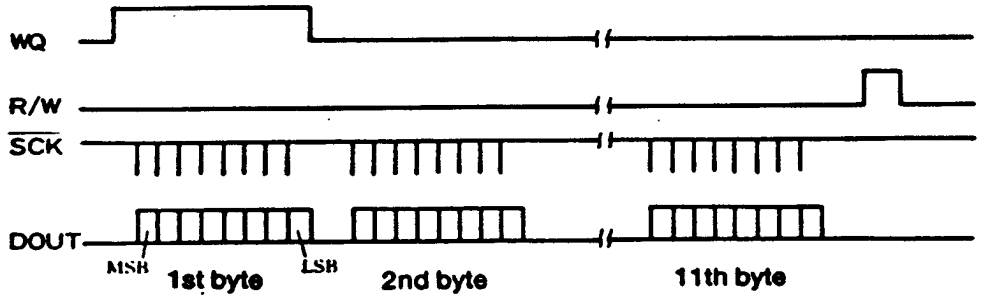
This interface is used to send the controller SPC internal status and Q-code data.

When it is confirmed that WQ has set to 1 in accordance with any of the conditions shown in the table below, outputing the clock signal to SCK allows the controller to obtain the data in bytes 1 through 11 of DOUT shown above.

Note that only the first byte need be read when only the internal status is required. (Although the play mute status is selected after completing track counting when track count mode is set, WQ does not set to 1 as the result of writing a new Q-code to the register. In this case, the mode should either be set to play mute, or the internal status register should be sampled to ascertain when NQ sets to 1.)

WQ sets to 1 when:

1.	The disc motor starts. The disk motor stops.
2.	When focused. When not focused.
3.	When a new Q-code is written to the register. (Never 1 during execution of a track count command)
4.	When track counting is completed.



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8. Controller Commands

R/W, DIN & $\overline{SCK}$ (Pins 36, 38 & 39)

Command List

Command	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Vol.	Bytes
STOP	0	0	0	×	0	0	0	0	0	1
FEED FORWARD	0	0	1	0	0	0	0	0	0	1
FEED RETURN	0	0	1	1	0	0	0	0	0	1
FOCUS START	0	1	0	×	0	0	0	0	0	1
DISC START	0	1	1	0	0	0	0	0	0	1
DISC BRAKE *1	0	1	1	1	0	0	0	0	0	1
PLAY	1	0	0	0	0	0	0	0	1	1
PLAY MUTE	1	0	0	1	0	0	0	0	0	1
FF *2	1	0	1	0	0	0	0	0	¼	1
FB *2	1	0	1	1	0	0	0	0	¼	1
FFF *2	1	1	0	0	0	0	0	0	¼	1
FFB *2	1	1	0	1	0	0	0	0	¼	1
SEARCH(PAUSE)	1	1	1	0	0	0	0	0	0	4
TRACK COUNT	1	1	1	1	0	0	0	0	0	4
INITIAL SET	0	0	0	0	1	0	0	0	0	1

The commands shown on the left can be used to control the SPC using the microcontroller. All of these commands with the exception of SEARCH and TRACK COUNT are 1-byte commands whose input is completed by inputing a single byte. The SEARCH and TRACK COUNT commands are 4-byte commands comprising the command and a 3-byte target value.

When the final DISK BRAKE event sets MZ to 1:

01110000 → 01110100

When ¼ volume is set to 0:

101*0000 → 101*1100
110*0000 → 110*1100

SEARCH Command

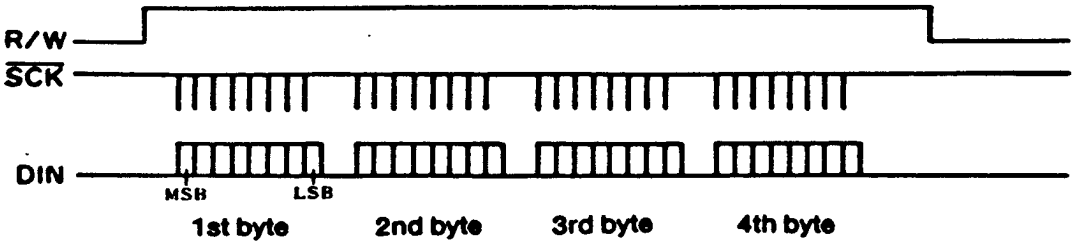
1	2	3	4
SEARCH	Minutes	Seconds	Frames

TRACK COUNT Command

1	2	3	4
TRACK COUNT	Number of tracks		0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
S	T_7	T_6	T_5	T_4	T_3	T_2	T_1	T_0	0	0	0	0	0	0	0

* No. of Tracks = $(1-2S) \times (2^7 * T_7 + 2^6 * T_6 + 2^5 * T_5 + 2^4 * T_4 + 2^3 * T_3 + 2^2 * T_2 + 2^1 * T_1 + T_0) * 128$
* Sign Bit S=0: Center to periphery
S=1: Periphery to center



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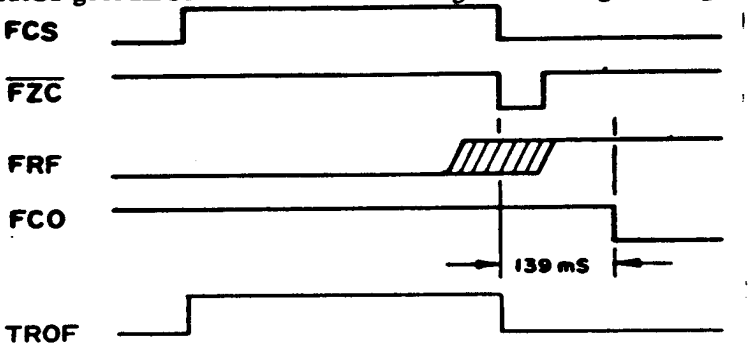
9. **Focus Servo**

FZC, FRF, FCS & TROF (Pins 14, 15, 13 & 19)

FZA, FRF and FCS are used to operate the focus servo. The FCS signal brings the pickup into focus. When the focal point is reached, the operation stops when an FZC signal is generated. The RFR signal detects the reflected light, and the FCO flag is dropped internally.

Note that TROF goes HIGH to turn off the tracking servo during focusing.



10. **Disc Servo**

- DM (Pin 12)

DM controls disc speed. This is a tri-state output, and output is in using PWM. The output signal is LOW during acceleration and HIGH during deceleration. The resolution for PWM is 1/147 (925ns) of 1 frame (136μs), with a maximum value of 128/147 (118μs).

Command	0.1	2	3−0	3−½	4−7·½			DUTY	Output Waveform
Mode	OFF	HOLD	ACC	BRK	ACC	AFC	PLL	DM Signal	
DM +			○			○	○	128/147	136μs, 118μs; 5 V, VH, 0 V
DM + (PWM)							○	1~127/147	MIN. 925ns; 5 V, VH, 0 V
Hi−Z	○	○	○	○	○	○	○	0	5 V, VH, 0 V
DM + (PWM)							○	1~127/147	5 V, VH, 0 V
DM −				○		○	○	128/147	5 V, VH, 0 V

Note: VH indicates high-impedence state

11. **Tracking Servo**

HF, TER, TROF, TRGL, TRGL, TRHD & KP (Pins 16, 17, 19, 20, 21 & 22)

Amplitude changes in the HF signal generated when tracks are traversed during searches are sampled at the zero point of the TER tracking error signal, and the TROF signal is output. The servo is switched ON/OFF according to the level of this signal.

Tracking is performed by outputing a HIGH- or LOW-level signal from the tri-state output KP. The TRDH signal goes HIGH during this interval and the tracking error signal is held. The TRGL signal is used to raise tracking gain after kick completion.

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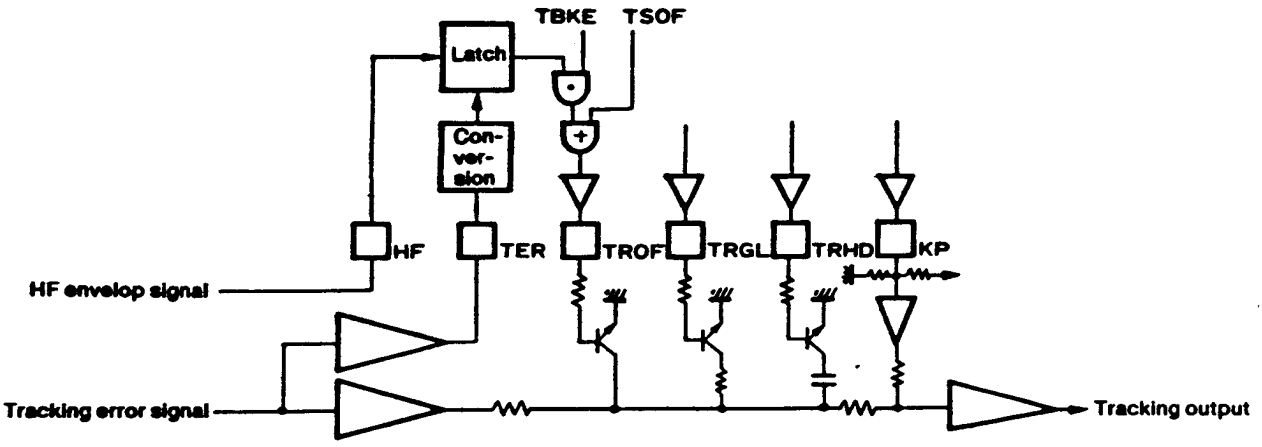

Command	0,1,2,3,4	5-0	5-½	6-0	6-½		
Pattern (Repeated during fast forward)	(Time: ms)	104	47.9	104	104		
TSOF TBKE TRGL TRHD KP							
Pattern (During searches the number of repeats depends on the time differential.)	(Time: ms)	.272 .544 7-1 174	.272 .544 7-4 7-5 174	.816 1.497 7-2 174	.816 1.497 7-6 174	2.993 5.714 7-3 348	2.993 5.714 7-7 348
Command Search Mode (Time differential in seconds)	7-0 (~+¼)	7-1 (+¼~4)	7-4 (~−¼) 7-5 (−¼~4)	7-2 (+4~128)	7-6 (−4~128)	7-3 (+128~)	7-7 (−128~)

Notes: 1. See separate diagram for 7½ command.
2. TSOF and TBKE are internal lines.

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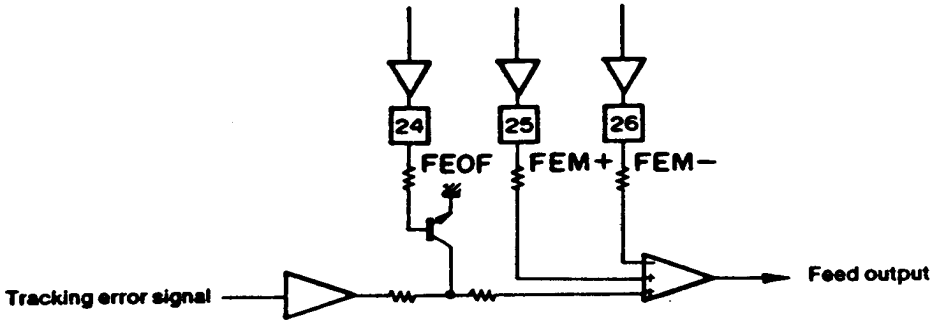
12. **Feed Servo**

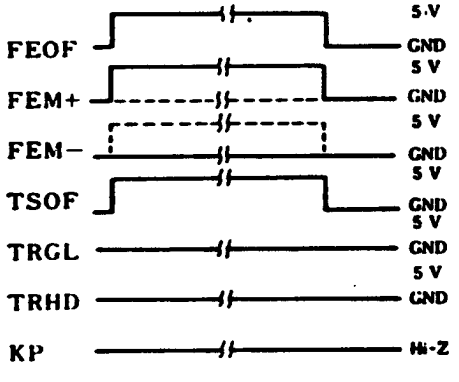
FEOF, FEM+, & FEM– (Pins 24, 25 & 26)

FEM+ and FEM– are output as high-speed feed signals. During this interval, FEOF is output to switch the feed servo off.



Command	0,2,3	1–0	1–½	4,5,6		
FEOF FEM+ FEM–						
Pattern (During searches the number of repeats depends on the time differential.)				(Time: ms)	34.8	34.8
Command Search Mode				7-0, 1, 2 7-4, 5, 6	7-3	7-7

13. **Track Count Command**



As shown on the left, each of the control signals are set when the track count command is executed. In this case, the TER signal is used to input of the track count signal, and its rising edges are integrated to form the count pulses. When the number of counts reaches the set value, the various control signals are reset to the same state as play mute.

Track counting can be aborted by inputing the required command after input of a count argument of 0.

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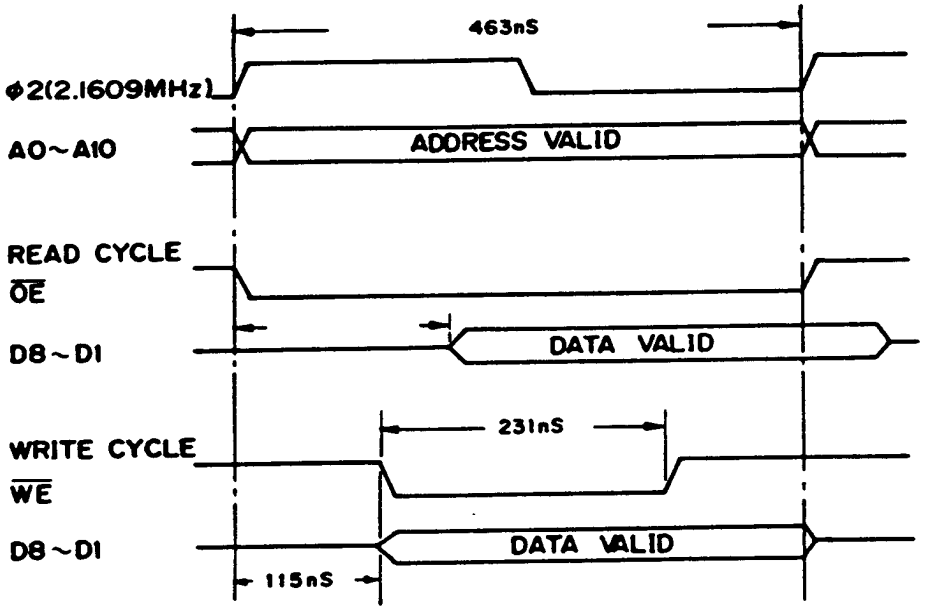
14. **RAM Interface**

A_0 to A_{10}, $\overline{WE}$, $\overline{OE}$, D_8 to D_1 (Pins 40, 42 to 50 & 53; 51; 52; and 54 to 61)

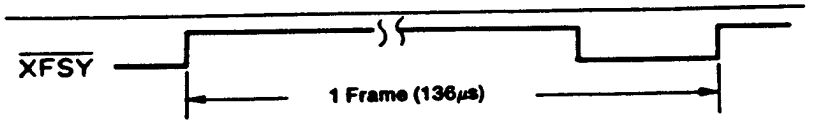
These are address, input/output control signals and data signals for the external RAM interface. SPC is in the output state when $\overline{WE}$ is LOW, and in the input state when it is HIGH.



15. **Clock Sync Signal**

(Pin 75)

7.35KHz frame sync signal.

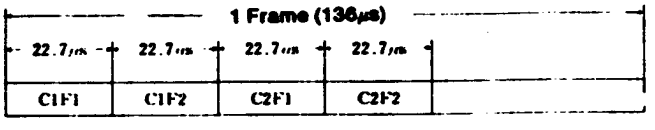


16. **C1 and C2 Error Correction Check Signal**

EFLG (Pin 73)

Check output pin that indicates the operating status of the C1 and C2 error correction circuit.

C1/C2	F2	F1
No errors	0	0
Single-error correction	0	1
Double-error correction	1	0
Correction impossible	1	1



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17. Data Control and Serial Signal Output

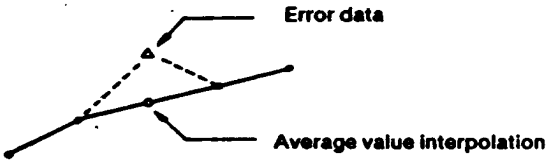
ϕ2, SDO, SDSY, SDSYMD, L/M, DTFLG, SAMPR & SAMPL (Pins 68, 66, 67, 65, 69, 63, 76 & 77)

ϕ2 is a 2.1609MHz crystal clock signal.

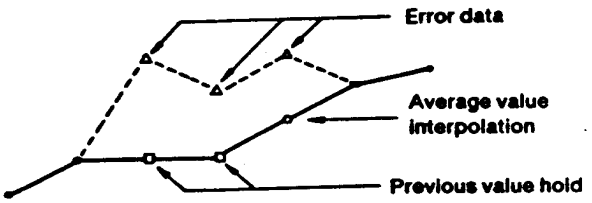
SDO is the DAC serial output signal for the ϕ2 bit rate. L/M is used to switch between MSB first and LSB first output to allow interfacing with various types of DAC and other digital devices.

DTFLG indicates whether the SDO data is correct, whether it has been interpolated, or whether it is previously held data, thereby reducing software overhead when the YM3616 is used in, for example, a CD-ROM system.

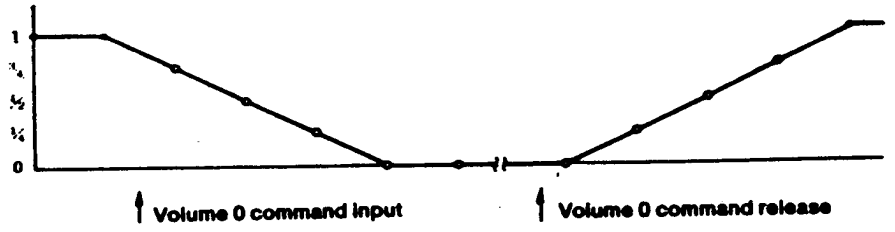
1. Single errors
(Left & right channels independent)



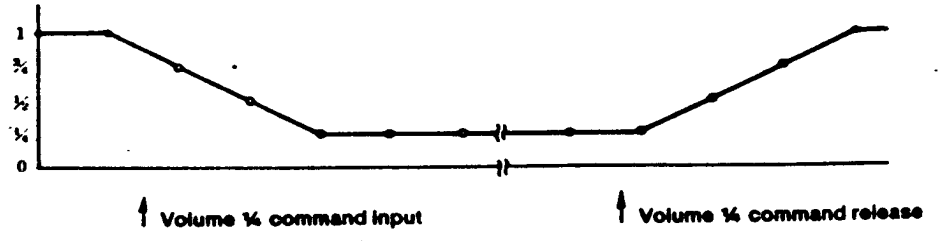
2. Consecutive errors
(Left & right channels independent)



3. Output at 0 volume command



4. Output at ¼ volume command



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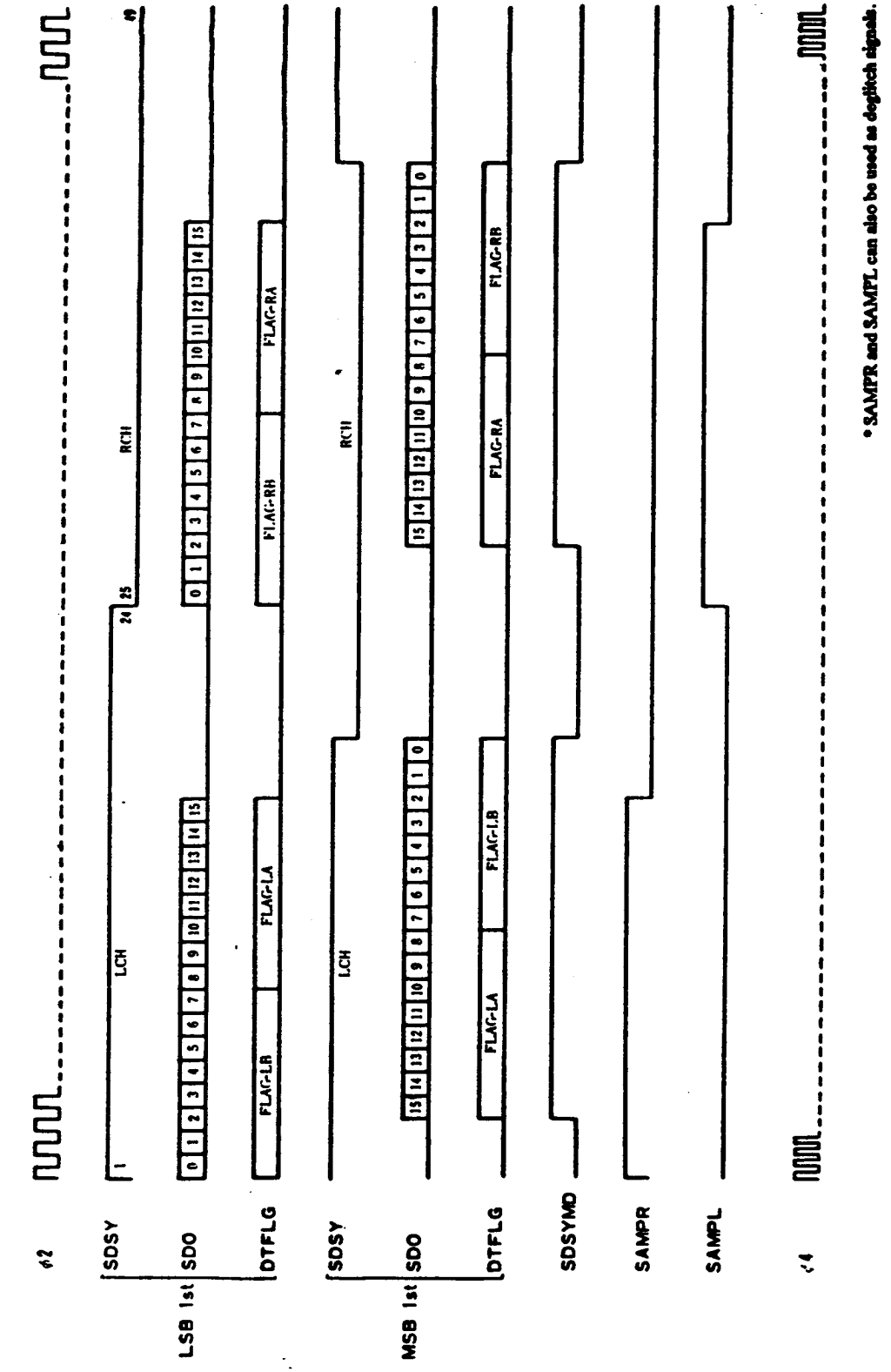
Audio Data Format



* SAMPR and SAMPL can also be used as deglitch signals.

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18. **De-Emphasis Signal**

    DEP (Pin 63)

    De-emphasis is required when the frequency characteristics control signal is HIGH.

19. **Test Pins**

    $\overline{\text{TEST IN}}$, $\overline{\text{TEST E}}$, $\overline{\text{TEST D}}$ & $\overline{\text{TCL}}$ (Pins 71, 70, 18 & 8)

    Normally not connected. Held HIGH using built-in pull-up resistors.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	−0.3 to +7.0	V
Input voltage	V_I	−0.3 to V_{DD}+0.5	V
Operating temperature	T_{OP}	−20 to +75	V
Storage temperature	T_{stg}	−50 to +125	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Rating			Unit
		min	typ	max	
Power supply voltage	V_{DD}	4.75	5.00	5.25	V
Operating temperature	T_{OP}	0	25	75	°C

ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0V ±5%)

Parameter	Symbol	Condition	Rating			Unit	Remarks
			min	typ	max		
Power supply current	I_{DD}	V_{DD}=5V		25	40	mA	
HIGH-level output voltage	V_{OH}	I_{OH}=20μA	4.0			V	
LOW-level output voltage	V_{OL}	I_{OL}=1mA			0.4	V	
HIGH-level input voltage (1)	V_{IH1}		3.5			V	See Note 1.
LOW-level input voltage (1)	V_{IH1}				1.5	V	See Note 1.
HIGH-level input voltage (2)	V_{IH2}		2.0			V	See Note 2.
LOW-level input voltage (2)	V_{IH2}				0.8	V	See Note 2.
Input leak current	I_{LK}	V_I=5V		10	μA		

Notes:

1. Applicable to Pins 3 (VCOI), 8 (EFMI), 14 ($\overline{\text{FZC}}$), 15 (FRF), 16 (HF) & 17 (TER).
2. Applicable to Pins 33 ($\overline{\text{RCK}}$), 38 (DIN), 39 ($\overline{\text{SCK}}$) & 54 to 61 (D_8 to D_1).

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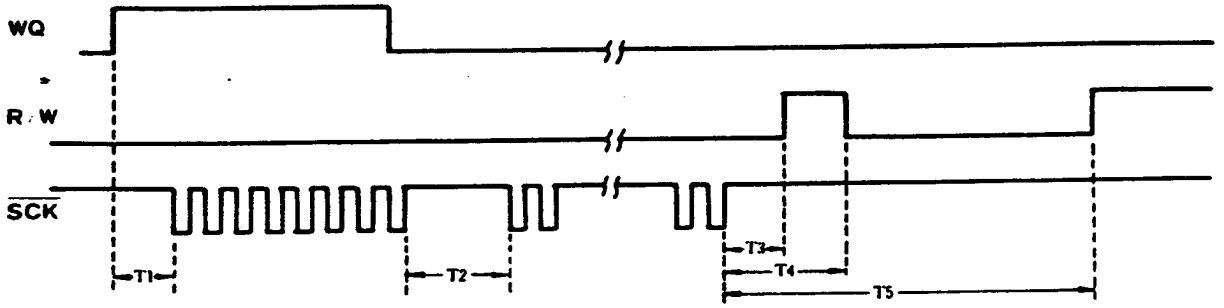
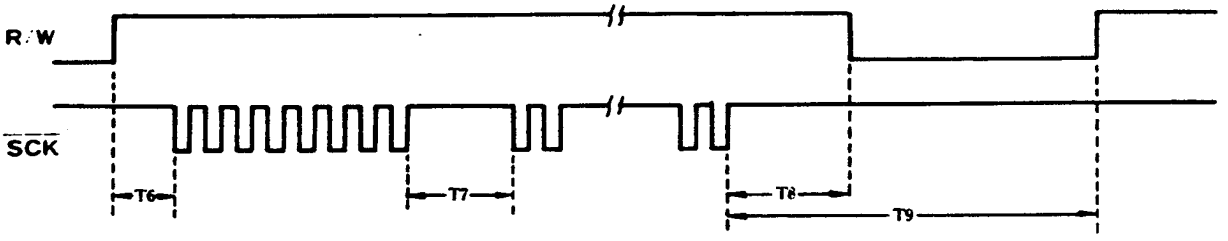
Microcontroller Interface Timing

1. SPC → Microcontroller



2. Microcontroller → SPC



3. $\overline{SPC}$ Timing



T1 T6	1μs or more	Momentary
T2 T7 T11	1μs or more	Random. When $\overline{SCK}$ is HIGH.
T10	1.2μ to 8μs or more	When SCK is LOW.
T8	12μs or more	Time after the last $\overline{SCK}$ goes HIGH.
T3	12μs to 135μs	
T4	13μs to 136μs	
T5 T9	408μs or more	

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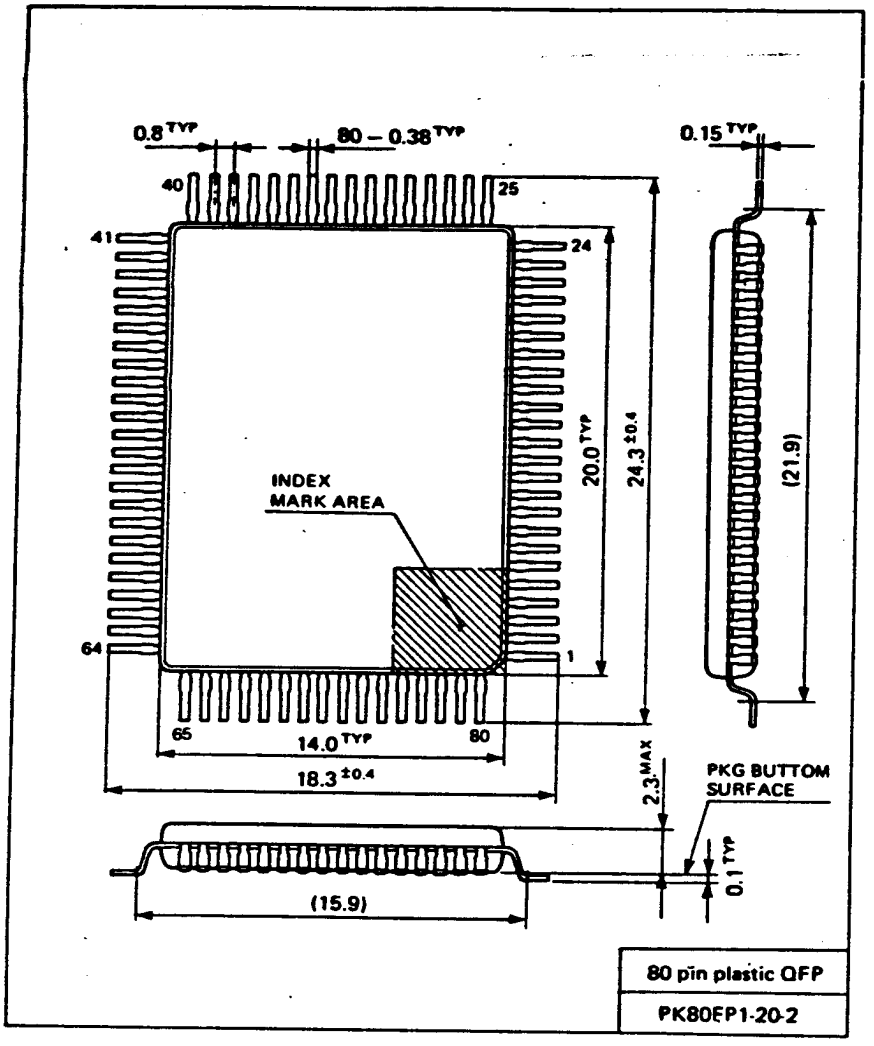
Package Dimensions



The specifications of this product are subject to improvement changes without prior notice.

AGENCY

YAMAHA CORPORATION
(Old Name: NIPPON GAKKI)

Address inquiries to:
Electronic System Division

- Toyooka Factory: 203, Matsunokijima, Toyooka-mura, Iwata-gun, Shizuoka-ken, 438-01 Electronic Equipment business section Tel. 053962-3125
- Tokyo Office: 3-4, Surugadai Kanda, Chiyoda-ku, Tokyo, 104 Ryumeikan Bldg. 4F Tel. 03-255-4481
- Osaka Office: 1-16, Shin-ashiyashimo, Suita-shi, Osaka, 565 Tel. 06-877-7731
- U.S.A.: YAMAHA International Corp. 6600 Orangethorp Ave. Buena Park California 90620

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